Amendments to the Specification:

Please replace paragraph [00112] with the following amended paragraph:

[00112] The video processing system 1400 includes several devices to be controlled by the scheduler host device 1428. These devices include MEC engine 1432, a compression engine 1436, a memory controller engine 1438, and the external host 1410. MEC engine 1432 includes a motion estimation and motion compensation array 1440, stream buffer 1442 and SRAM 1444. Compression engine 1436 includes a discrete cosine transform (DCT) and inverse DCT (IDCT) module 1446, a quantizer and dequantizer module 1448, a variable length coding (VLC) encoder 1450, and buffers such as block SRAMs 1452, 1454. Additional details of the video compression techniques for video processing system 1400 are disclosed in: (1) U.S. application Ser. No. [_____] 09/924,079, Attorney Docket 22682-6188, entitled "Cell Array and Method of Multiresolution Motion Estimation and Compensation," filed Aug. [[3]] 7, 2001, issued as U.S. Patent No. 6,970,509 on Nov. 29, 2005, the subject matter of which is hereby incorporated by reference in its entirety; and (2) U.S. application Ser. No. [_____] 09/924,140, Attorney Docket 22682-6189, entitled "DCT/IDCT With Minimum Multiplication," filed Aug. [[3]] 7, 2001, issued as U.S. Patent No. 7,035,332 on Apr. 25, 2006, the subject matter of which is hereby incorporated by reference in its entirety.